ANALOG DEVICES

HMC749LC3C

v06.0514

26 GHz, T FLIP-FLOP w/ RESET, PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

RoHS EARTH FRIENDLY

Typical Applications

The HMC749LC3C is ideal for:

- Serial Data Transmission up to 26 Gbps
- High Speed Frequency Divider (up to 26 GHz)
- Broadband Test & Measurement
- RF ATE Applications

Features

Supports Clock Frequencies up to 26 GHz

Differential & Single-Ended Operation

Fast Rise and Fall Times: 18 / 17 ps

Low Power Consumption: 270 mW typ.

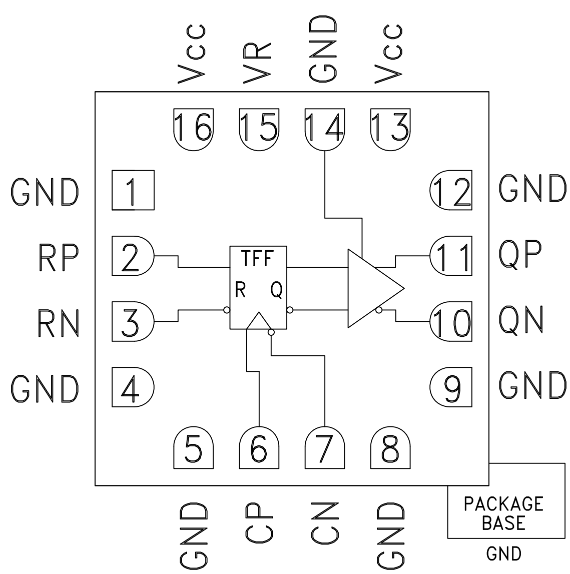
Programmable Differential
Output Voltage Swing: 600 - 1100 mV

Propagation Delay: 95 ps

Single Supply: 3.3 V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC749LC3C is a T Flip-Flop w/Reset designed to support clock frequencies as high as 26 GHz. During normal operation, with the reset pin not asserted, the output toggles from its prior state on the positive edge of the clock. This results in a divide-by-two function of the clock input. Asserting the reset pin forces the Q output low regardless of the clock edge state (asynchronous reset assertion). Reversing the clock inputs allows for negative-edge triggered applications.

All differential inputs to the HMC749LC3C are CML and terminated on-chip with 50 ohms to the positive supply, Vcc, and may be AC or DC coupled. The differential CML outputs are source terminated to 50 ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 ohm Vcc-terminated system, while DC blocking capacitors may be used if the terminating system is 50 ohms to ground. The HMC749LC3C also features an output level control pin, VR, which allows for loss compensation or signal-level optimazation. the HMC749LC3C operates from a single 3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vcc = 3.3 V, VR = 3.3 V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		3	3.3	3.6	V
Power Supply Current			82		mA
Maximum Clock Rate			26		GHz
Input Voltage Range		Vcc - 1.5		Vcc + 0.5	V
Input Differential Range		0.1		2	Vp-p

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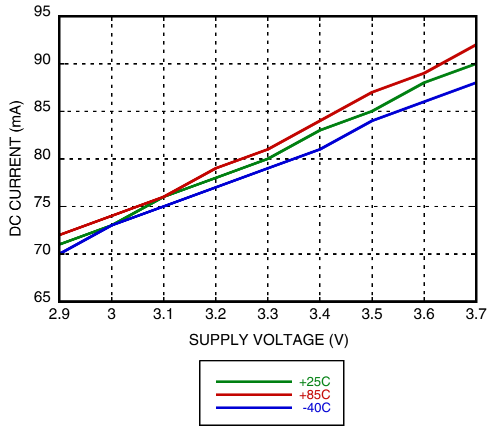
Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			3.29		V
Output Low Voltage			2.74		V
Output Rise / Fall Time	Differential, 20% - 80%		18 / 17		ps
Output Return Loss	Frequency <13 GHz		10		dB
Random Jitter Jr	rms [1]			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [2]		2		ps, p-p
Propagation Delay Clock to Q, td			95		ps
Propagation Delay Reset to Q, tdr			125		ps

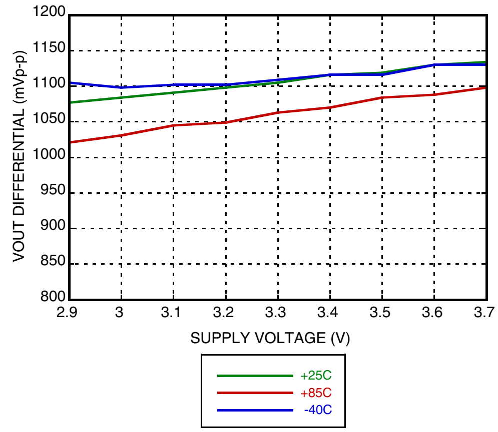
[1] Upper limit of random jitter, J_R, determined by measuring and integrating output phase noise with a sinusodal input at 5, 10, and 13.5 GHz over temperature.

[2] Deterministic jitter calculated by simultaneously measuring the jitter of a 200 mV, 12.5 GHz, 2^{15}-1 PRBS input and a single-ended ouput.

DC Current vs. Supply Voltage [1] [2]



Output Differential Voltage vs. Supply Voltage [1] [2]



[1] VR = +3.3 V [2] Frequency = 12 GHz

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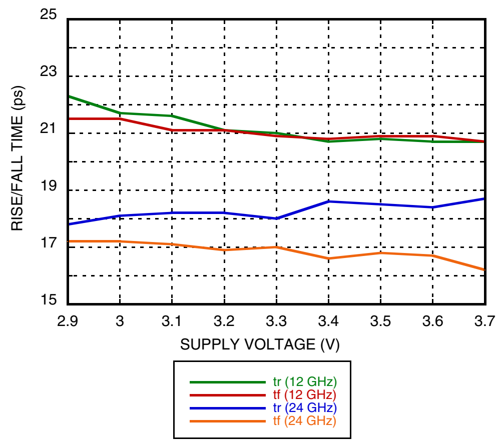
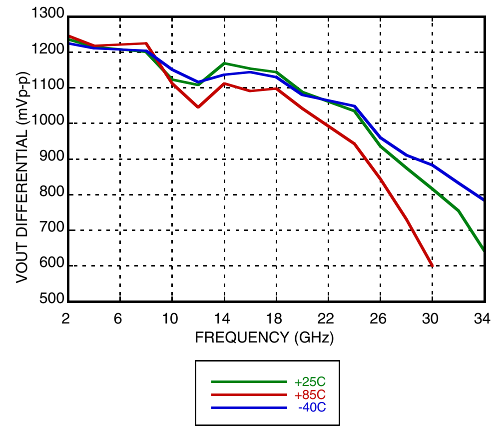
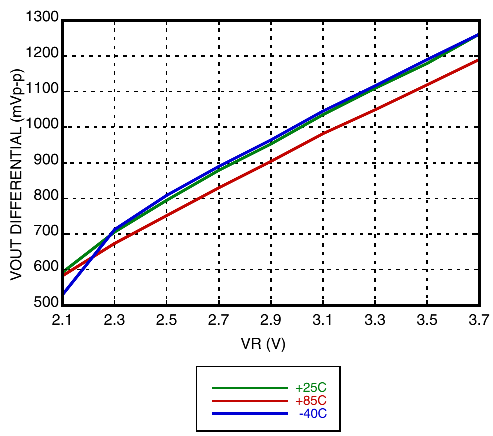
Rise / Fall Time vs. Supply Voltage [1] [3]



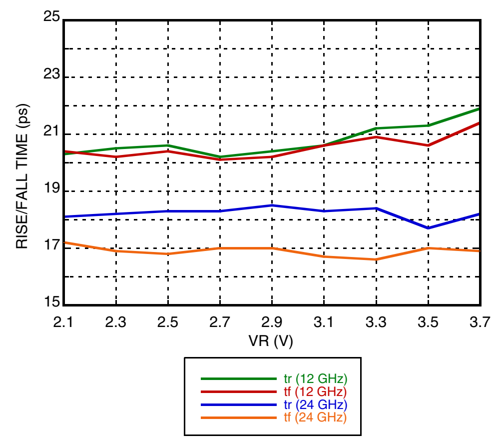
Output Differential Voltage vs. Input Frequency [1] [4]



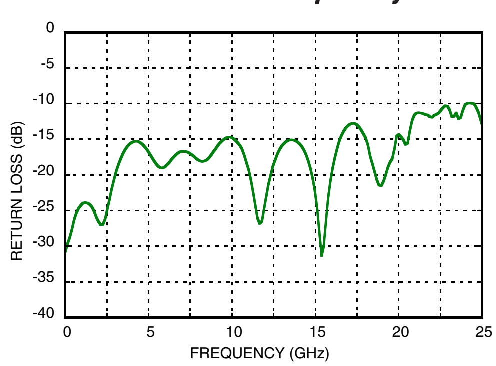
Output Differential Voltage vs. VR [1] [2]



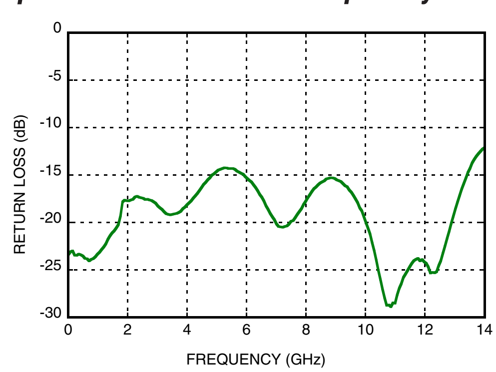
Rise / Fall Time vs. VR [1] [2]



Input Return Loss vs. Frequency

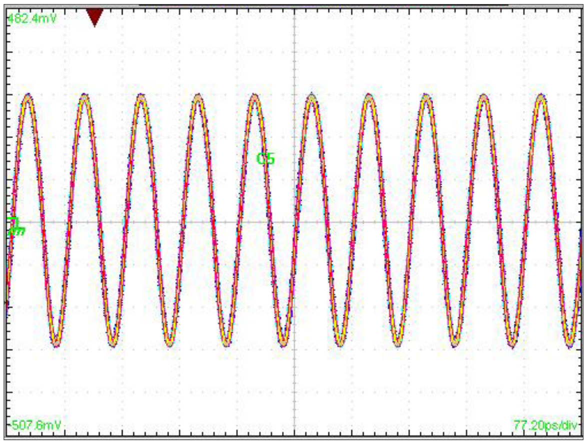


Output Return Loss vs. Frequency



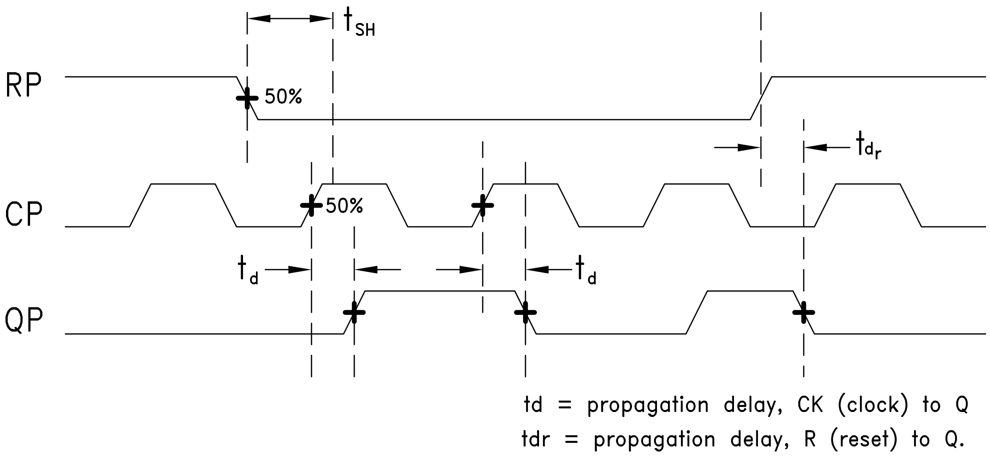
[1] VR = 3.3 V [2] Frequency = 12 GHz [3] Frequency = 24 GHz [4] Vcc = 3.3 V

Output Waveform



[1] Test Conditions:
Waveform generated with a CW signal source input at 26 GHz.
Diagram data presented on a Tektronix CSA 8000.
Device is AC coupled to scope.

Timing Diagram



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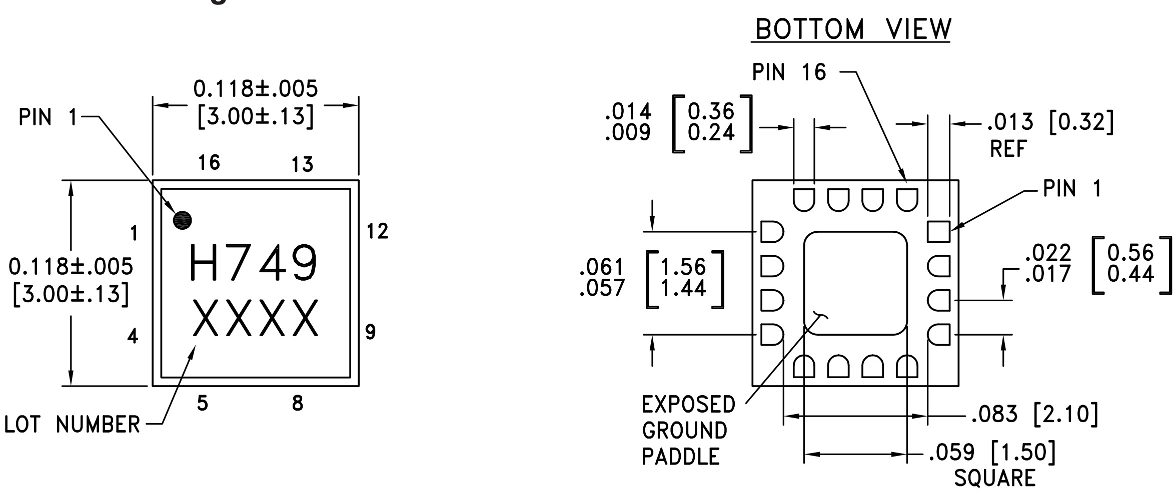
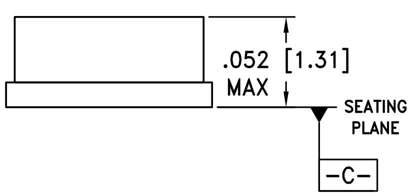
Absolute Maximum Ratings

Power Supply Voltage (Vcc)	Vcc -0.5 V to 3.75 V
Input Signals	Vcc - 2.0 V to Vcc + 0.5 V
Output Signals	Vcc - 1.5 V to Vcc + 0.5 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing





NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC749LC3C	Alumina, White	Gold over Nickel	MSL3 [1]	H749 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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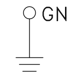
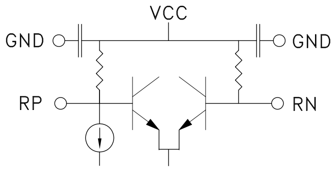
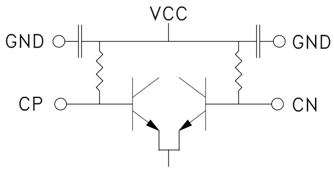
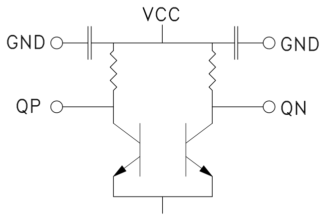
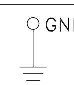
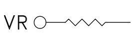
Pin Descriptions [1]

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	RP, RN	Differential Reset Inputs: Current Mode Logic (CML) referenced to positive supply.	
6, 7	CP, CN	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	QN, QP	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
13, 16	Vcc	Positive Supply	
14, Package Base	GND	Supply Ground	
15	VR	Output level control. Output level may be adjusted by applying a voltage to VR per "Output Differential vs. VR" plot.	

[1] Contact HMC for alternate pinouts

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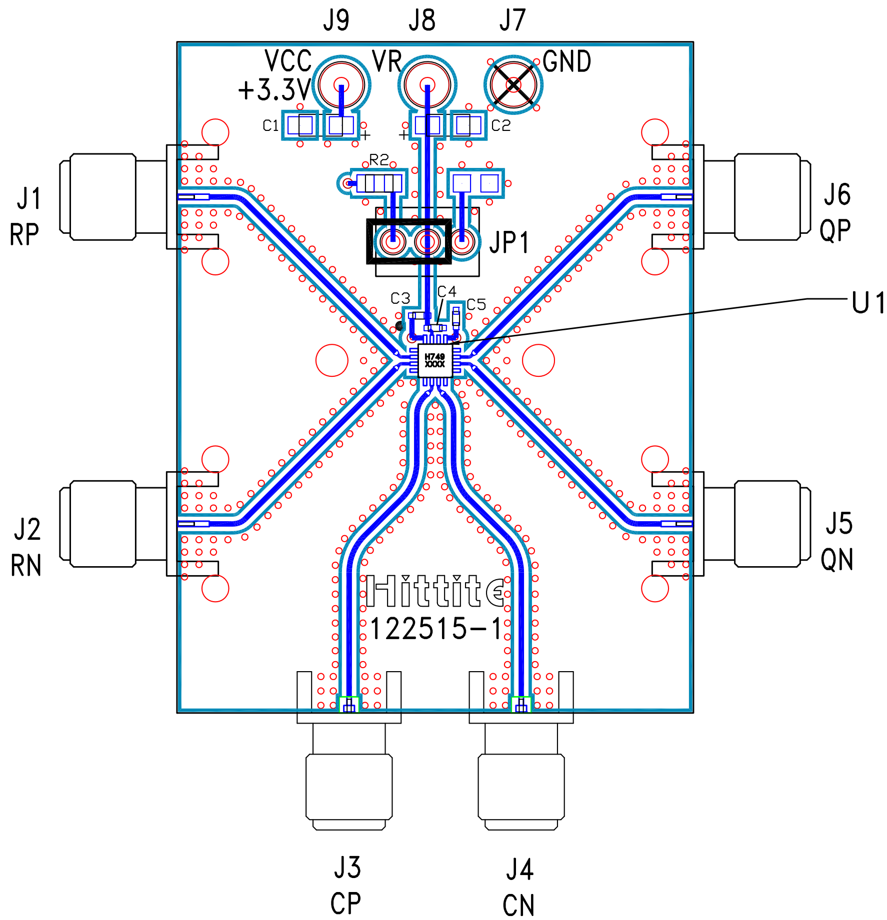
Evaluation PCB



List of Materials for Evaluation PCB 090-00328-00 [1]

Item	Description
J1, J2, J5, J6	PCB Mount SMA RF Connectors
J3, J4	SRI-K Connectors
J7 - J9	DC Pin
JP1	Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R2	10 Ohm Resistor, 0603 Pkg.
U1	HMC749LC3C
PCB [2]	122515 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package gro-und leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to Vcc for normal operation.

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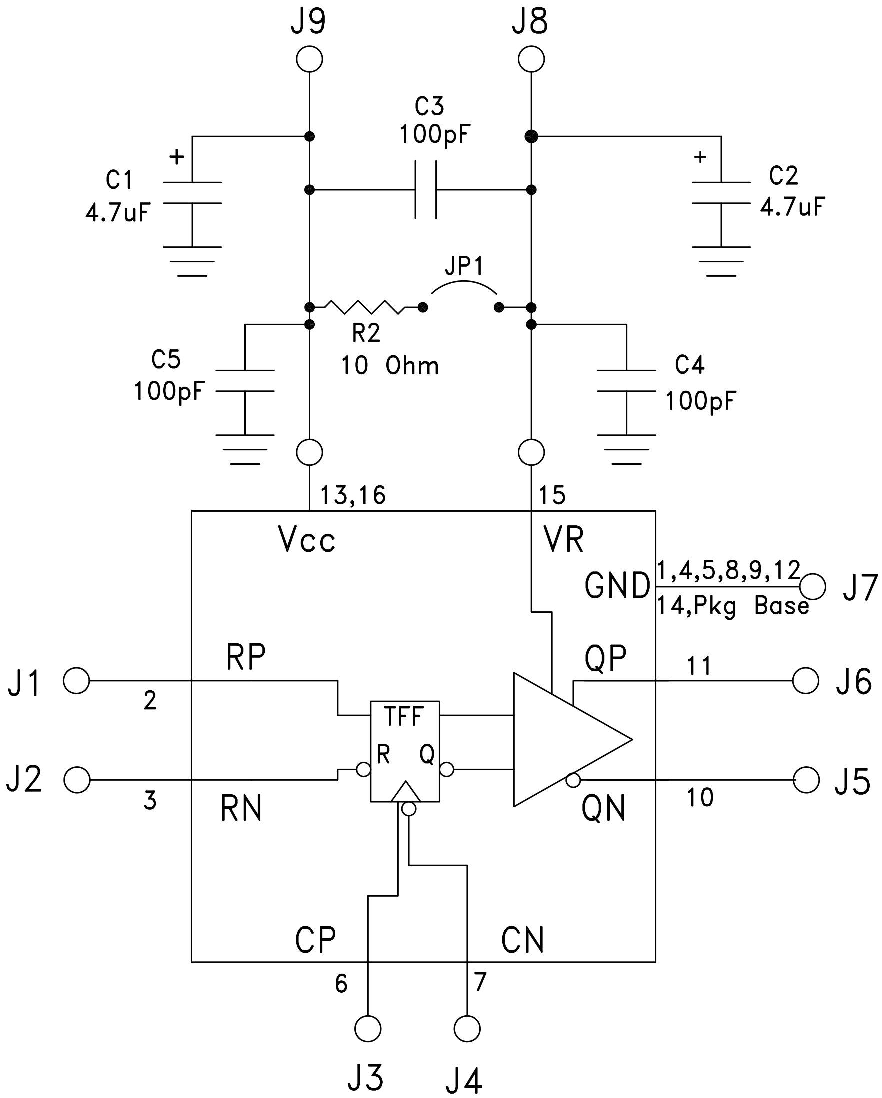
Application Circuit



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